

REMARKS

This Amendment is being filed in response to the Final Office Action mailed April 10, 2009, which has been reviewed and carefully considered. Reconsideration and allowance of the present application in view of the remarks to follow are respectfully requested.

Claims 1-3 and 5-16 remain in this application, where claims 1, 10 and 13 are independent.

In the Final Office Action, claims 1-2, 6 and 10-15 are rejected under 35 U.S.C. are rejected under 35 U.S.C. §103(a) over U.S. 2004/014894 (Cilvin) in view of a book entitled "Computer Organization and Design" (Hennessy). Claims 7-8 are rejected under 35 U.S.C. §103(a) over Cilvin and Hennessy in view of U.S. 6,624,818 (Mantor). Claim 16 is rejected under 35 U.S.C. §103(a) over Cilvin and Hennessy in view of an article entitled "Power Reduction through RTL Clock Gating" (Emnett). Claims 3, 5 and 9 are rejected under 35 U.S.C. §103(a) over Cilvin and Hennessy in view of common art/Official Notice. It is respectfully submitted that claims 1-3 and 5-15 are patentable over Cilvin, Hennessy,

Mantor, Emmett and Official Notice for at least the following reasons.

Cilvin is directed to a system that facilitates eliminating register usage for temporary operands involved in pipeline bypassing operations. During the pipeline bypassing operation, a processor examines an indicator associated with a series of instructions. If the indicator is set, the processor does not store the temporary operand used by the series of instructions into a register file of the processor, because the temporary operand will not be used by subsequent instructions. As correctly noted on page 3 of the Final Office Action, Cilvin does not disclose or suggest "wherein the result is passed to the functional unit via a bypass path before the storing of the result in the first register unit," as recited in independent claim 1, and similarly recited in independent claims 10 and 13. Page 499 of Hennessy is cited in an attempt to remedy the deficiencies in Cilvin.

Page 499 of Hennessy shows a block diagram referred to as FIGURE 6.51 which is described as follows:

Datapath for branch, including hardware to flush the instruction that follows the branch. This optimization moves the branch decision from the fourth

pipeline stage to the second; only one instruction that follows the branch will be in the pipe at that time. The control line IF.Flush turns the fetched instruction into a nop by zeroing the IF/ID pipeline register. Although the flush line is shown coming from the control unit in this figure, in reality it comes from hardware that determines if a branch is taken, labeled with an equal sign to the right of the registers in the ID stage. The forwarding muxes and paths must also be added to this stage, but are not shown to simplify the figure. (Emphasis added)

It is respectfully submitted that Page 499 of Hennessy merely describes a flush operation that zeros the pipeline register. It is respectfully submitted that such a disclosure has nothing to do, and does not disclose or suggest that a "result is passed to the functional unit via a bypass path before the storing of the result in the first register unit," as recited in independent claim 1, and similarly recited in independent claims 10 and 13.

Accordingly, it is respectfully requested that independent claims 1, 10 and 13, are allowable. In addition, claims 2-3, 5-9, 11-12 and 14-16 are also allowable at least because they depend from independent claims 1, 10 and 13, as well as for the separately patentable elements contained in each of the dependent claims. Accordingly, separate consideration of each of the dependent claims is respectfully requested.

For example, claim 7 recites that (illustrative emphasis provided):

the first register unit comprises a chain of registers for supplying bypass operand data, arranged as a shift register with an input coupled to a result output of the first one of the stages and operative to shift the result through successive shift register stages in successive instruction cycles, at least if storing of the result in the second register unit is disabled, the chain extending further than necessary for writing the result into the second register unit.

On pages 6-7 of the Final Office Action, it is correctly noted that Cilvin and Hennessy do not disclose or suggest these features. However, it is alleged that these features are disclosed on column 21, lines 29-32 of Mantor.

It is respectfully requested that column 21, lines 29-32 of Mantor merely describes storing results "based on a destination address 754" (column 21, lines 7-8), and a memory bypass register 760 that "stores the result generated by the first operation unit 710 to produce a first stored result. The first stored result is a time-delayed version of the result produced by the first operation unit." (Column 21, lines 33-37). As recited on column 21, lines 49-50, "the result is available on the output of the first memory bypass register 760 one clock cycle delayed." Column 21, lines 61-

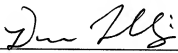
65 further recites that "if the memory 750 is relatively slow, multiple memory bypass registers may be included in a serial chain such that each additional memory bypass register produces a different time-delayed version of the results produced by the first operation unit 710." (Emphasis added)

Such a disclosure has nothing to do and does not disclose or suggest "if storing of the result in the second register unit is disabled, the chain extending further than necessary for writing the result into the second register unit," as recited in claim 7. Adding memory bypass registers if a memory is slow does not disclose or suggest extending a chain of registers of a first register unit if storing in a second register unit is disabled.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

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